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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,846	12/29/2003	Geun Il Lee	CU-3461 VE	6421

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,846	LEE, GEUN IL	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102(b)

3. The rejection of claims 1-12 as being anticipated by Sonoda et al. is ***maintained*** and repeated below with additions for the amended language.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sonoda et al.

6. Sonoda teaches the invention (claim 1) as claimed including a method for masking a postamble ringing phenomenon in a DDR SDRAM (e.g., see col. 2, lines 61-66), the method comprising the steps of:

a) storing data, which are applied from a memory controller, in a data input latch through a data buffer and aligning the stored data (e.g., see Figure 7 and col. 3, line 10 to col. 4, line 65);

b) controlling the data input latch so that the data stored in the data input latch do not change (e.g., see col. 2, lines 8-26);

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c) transmitting the data stored in the data input latch to a data input/output detection amplifier as sense amplifiers which are amplifier circuits for detecting and amplifying potential differences for data input/output, after a predetermined time delay with the predetermined time delay being inherently taught as all activity in the memory arrays is dependent upon clock signals with activities requiring one or more clock cycles, these time delays are predetermined as each type of memory activity requires at least a set time or number of cycles for signals and data to be transmitted (e.g., see col. 3, lines 10-25); and,

d) enabling the data input latch to receive new data after the data, which have been transmitted to the data input/output detection amplifier, are transmitted to a global input/output line (e.g., see col. 3, lines 10-63).

As to claim 2, Sonoda teaches in step b) an enable interval of a signal controlling the data input latch is adjusted so that the data stored in the data input latch do not change (e.g., see col. 4, lines 5-20).

As to claim 3, Sonoda teaches the signal, which controls the data input latch to prevent the data stored in the data input latch from changing, is generated by a signal which is synchronized with a falling edge of a DQS signal before it is generated (e.g., see col. 7, line 37 to col.8, line 24).

7. Sonoda teaches the invention (claim 4) as claimed including a method for masking a postamble ringing phenomenon in a DDR SDRAM (e.g., see col. 1, lines 22-34), the method comprising the steps of:

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a) storing data, which are applied as a signal received from a memory controller, in a data input latch through a data buffer and aligning the stored data (e.g., see Figure 7 and col. 3, line 10 to col. 4, line 65); and,

b) controlling the data input latch so that the data stored in the data input latch can maintain its data value before the data stored in the data input latch are transmitted to a global input/output line through a data input/output detection amplifier (e.g., see col. 2, lines 8-26) for a predetermined time delay with the predetermined time delay being inherently taught as all activity in the memory arrays is dependent upon clock signals with activities requiring one or more clock cycles, these time delays are predetermined as each type of memory activity requires at least a set time or number of cycles for signals and data to be transmitted;

As to claim 5, Sonoda teaches that after step b) a step of resetting the data input latch so as to revert to a state in which the data input latch can receive new data (e.g., see col. 3, line 64 to col. 4, line 49).

As to claim 6, Sonoda teaches that in step b) an enable interval of a signal controlling the data input latch is adjusted to prevent the data stored in the data input latch from changing during the predetermined time interval (e.g., see col. 4, lines 5-20).

8. Sonoda teaches the invention (claim 7) as claimed including a method for masking a postamble ringing phenomenon in a DDR SDRAM, the method comprising the steps of:

a) receiving a DQS signal through a DQS buffer, and receiving a plurality of data, including a first data and second data, through a data input buffer (e.g., see Figure 7);

b) storing the DQS signal outputted from the DQS buffer in a DQS latch (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39);

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c) generating a first signal synchronized with a rising edge of the DQS signal, and generating a second signal synchronized with a falling edge of the DQS signal (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39);

d) storing the first data from among the plurality of data outputted from the data input buffer in the data input latch synchronized with a rising edge of the first signal (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39);

e) storing the second data from among the plurality of data outputted from the data input buffer in the data input latch synchronized with a rising edge of the second signal (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39);

f) after a predetermined time interval with the a predetermined time interval being inherently taught as all activity in the memory arrays is dependent upon clock signals with activities requiring one or more clock cycles, these time intervals are predetermined as each type of memory activity requires at least a set time or number of cycles for signals and data to be transmitted, transmitting the first data and the second data, which are stored in the data input latch, to a data input/output detection amplifier, synchronized with a falling edge of the second signal (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39);

g) controlling operation of the data input latch by means of a control signal which is synchronized with the rising edge of the second signal in step e) and is then generated (e.g., see col. 11, line 17 to col. 12, line 30).

As to claim 8, Sonoda teaches operation of the DQS latch is masked while the control signal maintains an enabled state at a high level (e.g., see col. 8, line 38 to col. 9, line 32).

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As to claim 9, Sonoda teaches the control signal is disabled by a data in a strobe pulse signal which enables the data input/output detection amplifier (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39).

As to claim 10, Sonoda teaches a step of providing a ringing phenomenon mask section which generates the control signal synchronized with the rising edge of the second signal; that can adjust its own delay time, thereby adjusting an enable interval of the control signal (e.g., see Figure 7 and col. 2, line 61 to col. 3, line 39).

9. Sonoda teaches the invention (claim 11) as claimed including an apparatus for masking a postamble ringing phenomenon in a DDR SDRAM, the apparatus comprising:

a data strobe buffer for receiving a data strobe signal from a memory controller (e.g., see Figure 7);

a data strobe latch for latching the data strobe signal outputted from the data strobe buffer (e.g., see Figure 7);

a data buffer for receiving data applied from a memory controller (e.g., see Figure 7);

a data latch for latching the data outputted from the data buffer and for transmitting the latched data to a data input/output detection amplifier in response to an output signal received from the data strobe latch (e.g., see Figure 7);

a ringing phenomenon mask section for controlling the operation of the data latch in response to the output signal of the data strobe latch (e.g., see col. 2, lines 8-26).

As to claim 12, Sonoda teaches the data strobe signal is a clock signal, the ringing phenomenon mask section includes means to synchronize the control signal with a falling edge of the clock signal and generates the control signal thereafter, so that data transmission from the

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data buffer to the data latch is masked when the ringing phenomenon mask section is enabled (e.g., see col. 9, line 10 to col. 10, line 50).

RESPONSE TO APPLICANT'S REMARKS

10. Applicant's arguments filed September 28, 2006 have been fully considered but they are not persuasive.

11. As to remarks that the cites given are too extensive and there being a requirement on the part of the examiner *to identify the particular part of the reference upon which a patentability rejection is based, when the reference is complex*, such as the Sonoda reference, the Sonoda reference is no more complex than the present application. Additionally, the sections in which two columns or more were cited are in relationship to teaching claimed functionalities rather than easily identifiable apparatus elements.

12. The first limitation '*storing data, which are applied from a memory controller, in a data input latch through a data buffer and aligning the stored data,*' the reference teaches a memory array which stores data in a data buffer in different bit increments. The bits must be properly aligned in the rows and columns as they are stored. The section cited also discusses different control functionality applied to the memory arrays.

13. As to claim limitation (d) of claim 1, *'enabling the data input latch to receive new data after the data, which have been transmitted to the data input/output detection amplifier, are transmitted to a global input/output line,'* the reference discusses sense amplifiers which detect and amplify the data input/output to/from the arrays.

14. Figure 7 was also cited as being the apparatus for performing the claimed method steps.

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15. The limitations are all taught to the extent required by the actual claim language. Citing a single sentence is not required particularly when concepts and method steps are being described.

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONCLUSION

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Tuesday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Thursday, December 07, 2006

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